AMENDMENTS TO THE SPECIFICATION

At page 9 please replace the paragraph commencing at line 12 with the following amended paragraph:

Before transferring all 1-byte data bits (i.e., first program data bits) to the data register 220, the control logic 210 enables a control signal HV so that the high voltage generator 160 generates a high voltage required for a program operation in the memory 100. The control logic 210 detects a start bit and a stop bit of serial data SDA applied to the data pin 301. When the control logic 210 detects the start bit, the first program data bits of the data register 220 is loaded on a write buffer 180, and the address of the address register 230 is transferred to a row and column decoder block 120. At the same time, the control logic 210 enables the control signal PGM for performing the program operation of the first program data bits in the memory chip 100 for a predetermined time (e.g., 30 μs) according to a conventional method.

At page 11 please replace the paragraph commencing at line 11 with the following amended paragraph:

If the time (e.g., 30 μs) for programming data in the memory is not beyond a current driving capability of a high voltage generation block 160t, the time is constant regardless of the size of the programmed data. Therefore, 4-byte data can be transferred within predetermined time, as shown in FIG. 3. A data transfer speed for transferring data to the data register 220 in this case increases more than that in a nonvolatile memory having 1-byte capacity. If the data transfer speed is determined on the basis of a nonvolatile memory having the longest programming time, such a transfer can be applied

to all nonvolatile memories. That is, data transfer and program operations may be performed by the same manner irrespective of a transfer data size (or write buffer size).